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EXAMINER	
MARTIN, LAURA E	

ART UNIT	PAPER NUMBER
2853	

NOTIFICATION DATE	DELIVERY MODE
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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## Office Action Summary

Application No.

10/827,142

Applicant(s)

BENJAMIN, TRUDY L.

Examiner

Laura E. Martin

Art Unit

2853

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10/17/07.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 9-34 and 58-63 is/are pending in the application.
- 4a) Of the above claim(s) 9-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 23-34 and 58-63 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                            |                                                                                         |
|------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                           | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23-25, 58 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schloeman et al (US 6659581 B2) in view of Wade et al. (US 6290333 B1).

**Schloeman et al. disclose the following claim limitations:**

As per claim 23: an address generator (figure 4 - the bank circuitry (elements 110a/b and 118 a/b) generate address signals (FIRE\_PULSE 1/2) from the bits received from the ADDRESS\_BUS.) including first bank circuitry (figure 4, elements 110a and 118a) configured to receive a first group of timing pulses from a series of timing pulses and generate a first sequence of address signals in response to the first group of firing pulses, wherein the first sequence of address signals is adapted to enable the fluid ejection elements (figure 4, FIRE\_PULSE 1); and second bank circuitry (figure 4, elements 110b and 118b) configured to receive a second group of timing pulses from the series of timing pulses and generate a second sequence of address signals in response to the second group of timing pulses, wherein the second sequence of address signals is adapted to enable the fluid ejection elements (figure 4, FIRE\_PULSE 2).

As per claim 24: a first shift register to provide first output signals (figure 4, element 110a and 116a).

As per claim 25: a second shift register configured to provide output signals (figure 4, elements 110b and 116b)

As per claim 58: an address generator (figure 4 - the bank circuitry (elements 110a/b and 118 a/b) generate address signals (FIRE\_PULSE 1/2) from the bits received from the ADDRESS\_BUS.) electrically coupled to resistors, the address generator including: first bank circuitry (figure 4, elements 110a and 118a) configured to receive a first group of timing pluses and generate a first sequence of address signals (figure 4, FIRE\_PULSE 1) in response to the first group of timing pulses, the first bank circuitry electrically connected to the resistors, wherein the first sequence of address signals is adapted to enable the resistors to conduct (column 2, lines 31-41); and second bank circuitry (figure 4, elements 110b and 118b) configured to receive a second group of timing pulses and generate a second sequence of address signals (figure 4, FIRE\_PULSE 2) in response to the second group of timing pulses, the second bank circuitry electrically connected to the resistors, wherein the second sequence of address signals is adapted to enable the resistors to conduct (column 2, lines 31-41).

As per claim 63: the first bank circuitry is a first bank generator and the second bank circuitry is a second bank generator (bank generator is not defined, but both bank circuitries generate signals as explained above).

**Schloeman et al. do not disclose the following claim limitations:**

As per claim 23: firing cells including a first group of fluid ejection elements and a second group of fluid ejection elements.

As per claim 58: a first group of resistors and a second group of resistors.

**Wade et al. disclose the following claim limitations:**

As per claim 23: firing cells including a first group of fluid ejection elements and a second group of fluid ejection elements (figure 2b, element 90).

As per claim 58: a first group of resistors and a second group of resistors (figure 2b, element 90).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection device taught by Schloeman et al. with the disclosure of Wade et al. in order to provide a higher quality control device for colored printing.

Claims 26, 59, and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schloeman et al (US 6659581 B2) and Wade et al. (US 6290333 B1), and further in view of Kanematsu et al. (US 20020113832 A1).

**Schloeman et al. as modified disclose the following claim limitations:**

The invention of claims 23 and 58.

**Schloeman et al. disclose the following claim limitations:**

As per claim 59: a first shift register to provide first output signals (figure 4, element 110a and 116a).

As per claim 60: a second shift register configured to provide output signals  
(figure 4, elements 110b and 116b)

**Schloeman et al. as modified do not disclose the following claim limitations:**

As per claim 26: the first bank circuitry comprises a first logic circuit configured to provide the first sequence of address signals based on the first output signals and the second circuitry comprises a second logic circuit configured to provide the second sequence of address signals based on the second output signals.

As per claim 59: a first logic circuit configured to provide the first sequence of address signals based on the first outputs.

As per claim 60: a second logic circuit configured to provided the second sequence of address signals based on the second output signals.

**Kanematsu et al. disclose the following claim limitations:**

As per claim 26: the first bank circuitry comprises a first logic circuit configured to provide the first sequence of address signals based on the first output signals and the second circuitry comprises a second logic circuit configured to provide the second sequence of address signals based on the second output signals[0210].

As per claim 59: a first logic circuit configured to provide the first sequence of address signals based on the first outputs [0210].

As per claim 60: a second logic circuit configured to provided the second sequence of address signals based on the second output signals [0210].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection apparatus taught by Schloeman et al. as modified

with the disclosure of Kanematsu et al. in order to provide independent printing to each printhead.

Claims 27-34, 61 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schloeman et al (US 6659581 B2) and Wade et al. (US 6290333 B1), and further in view of Bloomberg (US 20020097287 A1).

**Schloeman et al. as modified disclose the following claim limitations:**

The invention of claims 23 and 58.

**Schloeman et al. as modified do not disclose the following claim limitations:**

As per claim 27: a direction circuit configured to receive a third group of timing pulses from the series of timing pulses and provide direction signals in response to the third group of timing pulses.

As per claim 28: the first shift register and the second shift register receive the direction signals and shift in selected direction based on the direction signals.

As per claim 29: a first logic circuit configured to provide the first sequence of address signals in response to the first output signals.

As per claim 30: a first logic circuit configured to receive a first sequence of address signals in response to the first group of timing pulses.

As per claim 31: a direction circuit configured to receive a third group of timing pulses and provide direction signals in response to the third group of timing pulses.

As per claim 32: the first bank circuitry and the second bank circuitry receive the direction signals and provide the first sequence of address signals and the second

sequence of address signals in selected sequences based on the direction signal pulses.

As per claim 33: the first bank circuitry is a first bank generator and the second bank circuitry is a second bank generator.

As per claim 34: the address generator is electrically coupled to both the first group of fluid ejection elements and the second group of fluid ejection elements, wherein the first bank circuitry is coupled to the first group of fluid ejection elements and not the second group of fluid ejection elements, and wherein the second bank circuitry is coupled to the first group of fluid ejection elements and not the second group of fluid ejection elements.

As per claim 61: a direction circuit configured to receive a third group of timing pulses from the series of timing pulses and provide direction signals in response to the third group of timing pulses.

As per claim 62: the second shift register receives the direction signals and shift in a selected direction based on the direction signals.

**Bloomberg discloses the following claim limitations:**

As per claim 27: a direction circuit configured to receive a third group of timing pulses from the series of timing pulses and provide direction signals in response to the third group of timing pulses ([0037, figure 5B, figure 4, elements 74, 46, and 66).

As per claim 28: the first shift register and the second shift register receive the direction signals (figure 6, element 90 and 92) and shift in selected direction based on the direction signals.



As per claim 29: a first logic circuit configured to provide the first sequence of address signals in response to the first output signals (figure 6, element 106).

As per claim 30: a first logic circuit configured to receive a first sequence of address signals in response to the first group of timing pulses (figure 6, element 106, figure 4).

As per claim 31: a direction circuit configured to receive a third group of timing pulses and provide direction signals in response to the third group of timing pulses ([0037, figure 5B, figure 4, elements 74, 46, and 66).

As per claim 32: the first bank circuitry and the second bank circuitry receive the direction signals and provide the first sequence of address signals and the second sequence of address signals in selected sequences based on the direction signal pulses ([0037-0038], figure 5B, figure 4, elements 74, 46, and 66).

As per claim 33: the first bank circuitry is a first bank generator and the second bank circuitry is a second bank generator (figures 4 and 6, elements 64 and 66 generate printing from inkjets 46).

As per claim 34: the address generator is electrically coupled to both the first group of fluid ejection elements and the second group of fluid ejection elements (figure 4, elements 62 and 46), wherein the first bank circuitry is coupled to the first group of fluid ejection elements and not the second group of fluid ejection elements, and wherein the second bank circuitry is coupled to the first group of fluid ejection elements and not the second group of fluid ejection elements (figures 4 and 6).

As per claim 61: a direction circuit configured to receive a third group of timing pulses from the series of timing pulses and provide direction signals in response to the third group of timing pulses ([0037], figure 5B, figure 4, elements 74, 46, and 66).

As per claim 62: the second shift register receives the direction signals and shift in a selected direction based on the direction signals (figure 6, element 90 and 92; [0023])

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the fluid ejection apparatus taught by Schloeman et al. as modified with the disclosure of Bloomberg in order to improve printing and image quality.

### ***Response to Arguments***

Applicant's arguments filed 10/17/07 have been fully considered but they are not persuasive.

Applicant argues that there is no address generator; however, the examiner disagrees. The bank circuitry (elements 110a/b and 118 a/b) generate two sets of address signals (FIRE\_PULSE 1 and FIRE\_PULSE 2) from the bits received from the ADDRESS\_BUS.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura E. Martin whose telephone number is (571) 272-2160. The examiner can normally be reached on Monday - Friday, 7:00 - 3:30.


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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen D. Meier can be reached on (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Laura E. Martin

  
MANISH S. SHAH  
PRIMARY EXAMINER  
1/18/08